SYLVANIA

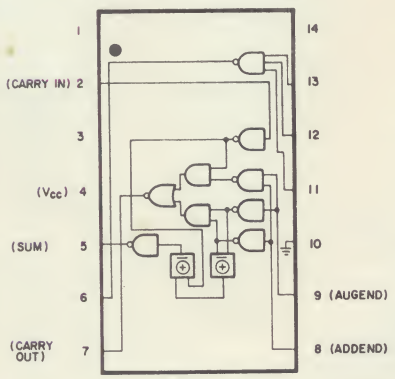
INTEGRATED CIRCUITS

NEW PRODUCT REPORT

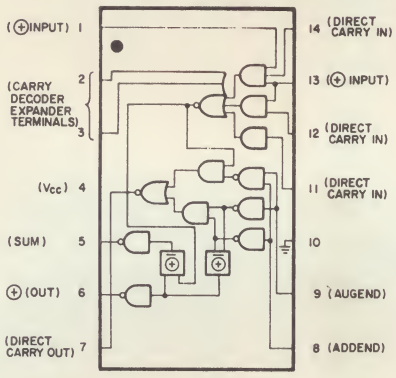
Fast Adder SM10, SM20 SM30, SM40 Series

monolithic digital functional arrays

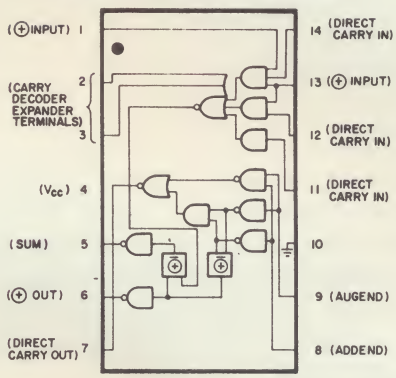
SM-10 SERIES FULL ADDER



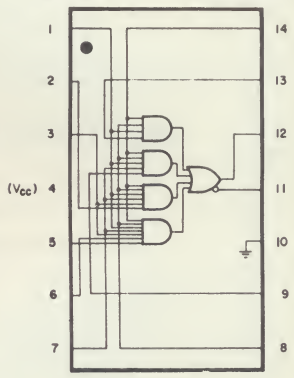
SM-20 SERIES
DEPENDENT CARRY FAST ADDER

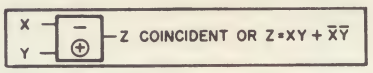


SM-30 SERIES
INDEPENDENT CARRY FAST ADDER



SM-40 SERIES CARRY DECODER





FUNCTIONAL DESCRIPTION:

The fast adder family of Monolithic Digital Functional Arrays is a new group of Integrated Circuits from Sylvania which implement high speed adder subsystems with both anticipated carry and ripple carry configurations.

The basic fast adder circuit is interconnected with standardized metalizations to form three single adder subsystems: the SM30 series independent-carry fast adder, the SM20 series dependent-carry fast adder, and the SM10 series full adder.

Within an adder subsystem, the SM30 series permits parallel addition with simultaneous carry of both "1" and "0". For anticipated carry beyond four stages, the SM40 decoder package is used between each SM30 stage to extend anticipated carry for as many stages as required.

The SM20 dependent-carry fast adder on the other hand is logically arranged to permit simultaneous carry of ones only. Zero will be carried only after the prior carry is cleared. With an SM20 at the beginning and end of each eight adder stages, carry lines can be truncated at each eighth stage for reinitiation at the start of the next eight stages, or end-around-carried to the adders least significant stage.

This approach increases reliability through fewer packages and interconnections and improves system economy by permitting use of standard I/C packaging formats (14-lead plug-in package and TO-85 flat pack).

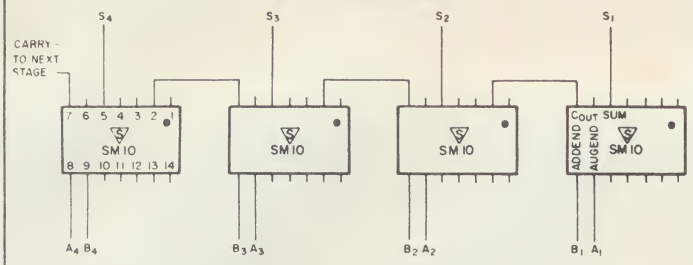
For example, using the SM20 and SM30 series fast adder in conjunction with the SM40 decoder package, a 64 stage adder subsystem capable of adding two 64-digit binary numbers in less than 200 ns, can be built with only 96 of these packages.

Where system specifications stipulate ripple carry adder subsystems, the SM10 series full adder can be used to advantage. With this device, package count is reduced to one package per stage with a commensurate reduction in interconnections. As an example, a 64-stage ripple carry adder subsystem built with this circuit can add two 64-digit numbers in less than a microsecond.

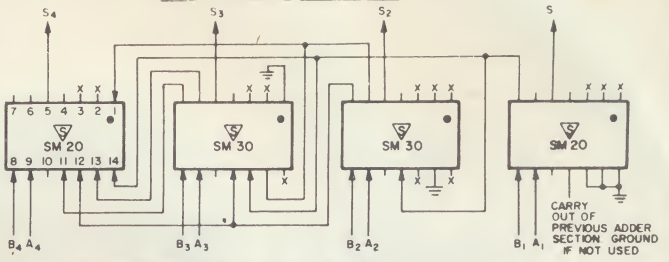
Throughout this discussion, a 64-stage adder has been used as an example of a large adder subsystem. The use of this example however does not imply any limit to the size of adder subsystems which can be developed with these arrays. The only known limits to adder subsystem size are those imposed by the particular system.

The purpose of this report is to provide tentative engineering data on new Sylvania Integrated Circuits.

"N" BIT RIPPLE CARRY ADDER



4 BIT ANTICIPATED CARRY ADDER



X = NO CONNECTION PIN 4 = V_{CC}, PIN 10 = GROUND

NOTE:
ALL SM30'S CAN BE USED, HOWEVER BY USING SM20'S AT THE BEGINNING AND END "ONES" COMPLEMENT AND END AROUND CARRY OPERATIONS CAN BE DONE

SPECIAL FEATURES:

- Implements anticipated carry, ripple carry, and serial adder subsystems.
- Simultaneous anticipated carry for up to eight stages.
- Carry lines truncated between each eight stages.
- One package per stage for ripple adder subsystems.
- 1.5 packages per stage for anticipated carry adders larger than eight stages.
- Full adder package has internal 3-input NAND gate for total arithmetic capability.
- Extremely fast add time.
- Single sided input and output.
- Saturated logic.
- Single 5-volt power supply.
- Excellent noise immunity.
- High logic levels.
- Low power consumption.
- Complete SUHL compatability.
- Complete compatibility with other logic forms (DTL, TTL).
- Available in 14-lead dual in-line plug-in package and TO-85 flat pack.

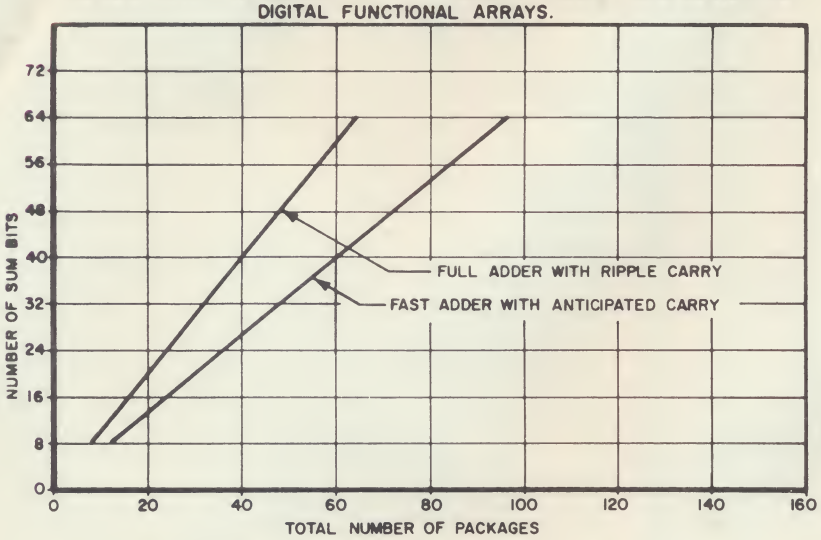
PERFORMANCE CHARACTERISTICS:

CHARACTERISTICS	TYPICAL VALUES
Propagation delay	Input to sum out 22 ns Input to carry out 10 ns
Power Dissipation	SM 10 - 90 mw per stage SM 20, SM30 - 125 mw per stage SM 40 - 25 mw per stage
Power Supply	5 volts DC
Noise Immunity	± 1 volt
Input Terminal "0" unit load "1" unit load	 1.33 ma 100 ua
Output logic "0" level	0.25 volts
Output logic "1" level	3.3 volts
Operating temperature	-55°C to +125°C(SM10, 11; SM20, 21; SM30, 31; SM40, 41) 0°C to +75°C (SM12, 13; SM22, 23; SM32, 33; SM42, 43)

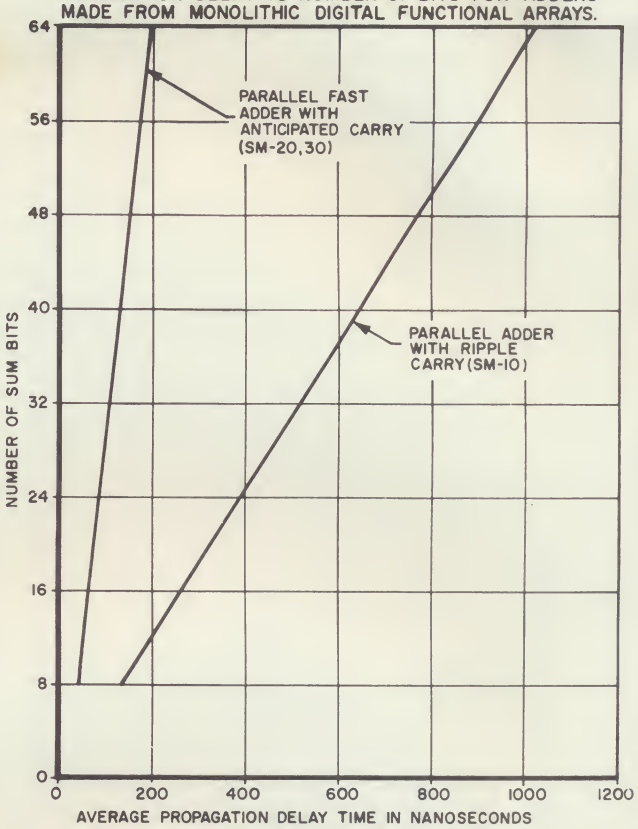
APPLICATION AREAS:

- Anticipated-carry fast parallel adder subsystems for large and small digital computer arithmetic sections.
- Ripple-carry parallel adder subsystems for large and small digital computer arithmetic sections.
- Serial adder subsystems for digital computers.
- Desk top calculators.
- Digital communication systems.
- Digital-graphic display systems.
- Process control systems.
- Numerical tool control systems.

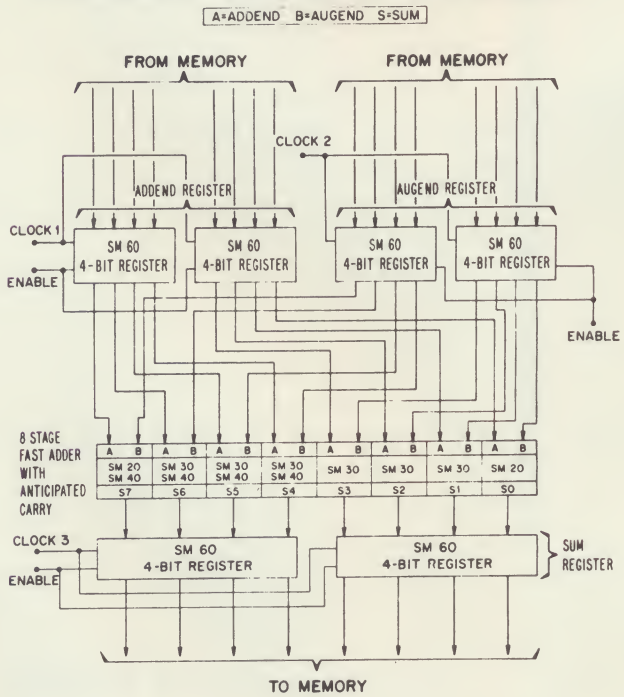
PACKAGE COUNT vs NUMBER OF BITS FOR ADDER MADE FROM MONOLITHIC DIGITAL FUNCTIONAL ARRAYS.

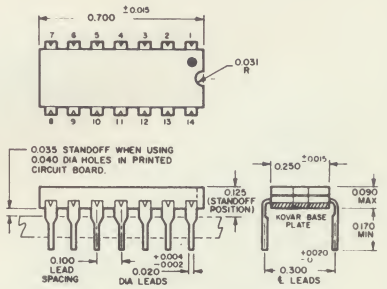


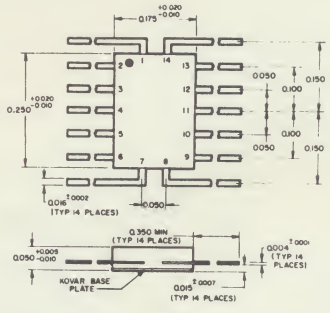
PROPAGATION DELAY vs NUMBER OF BITS FOR ADDERS MADE FROM MONOLITHIC DIGITAL FUNCTIONAL ARRAYS.



EIGHT STAGE CENTRAL COMPUTER ARITHMETIC SECTION IN 18 PACKAGES

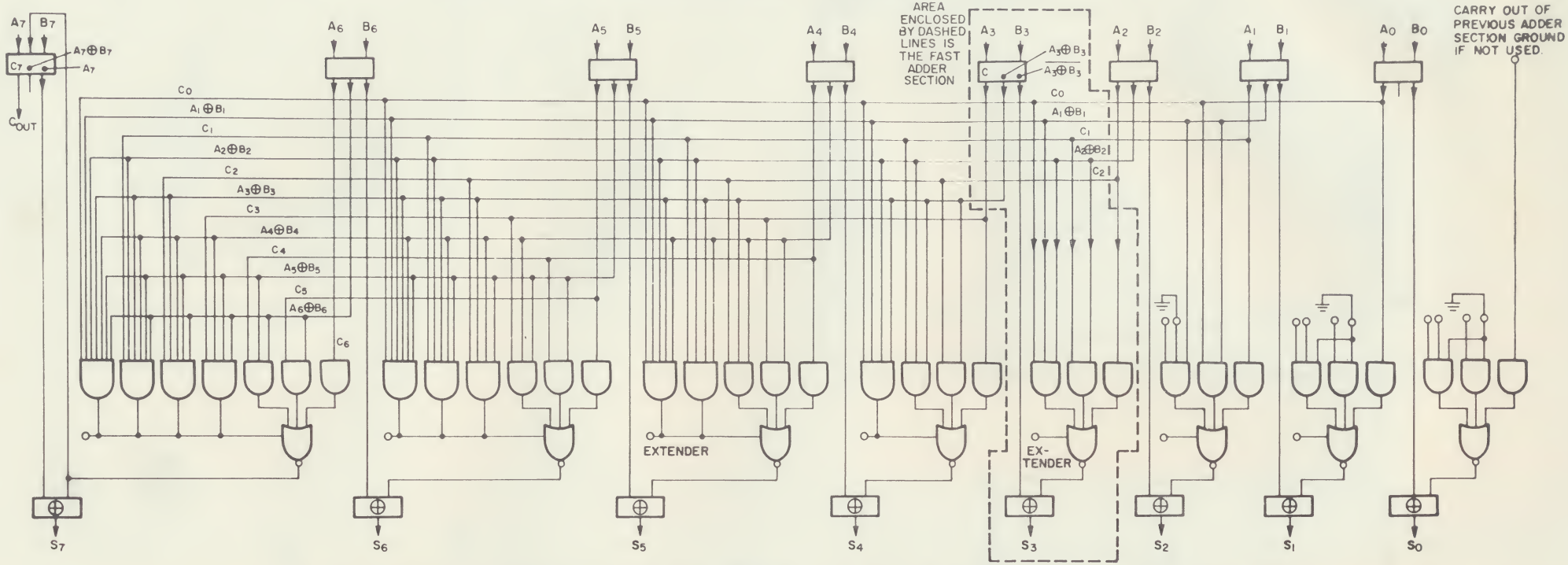




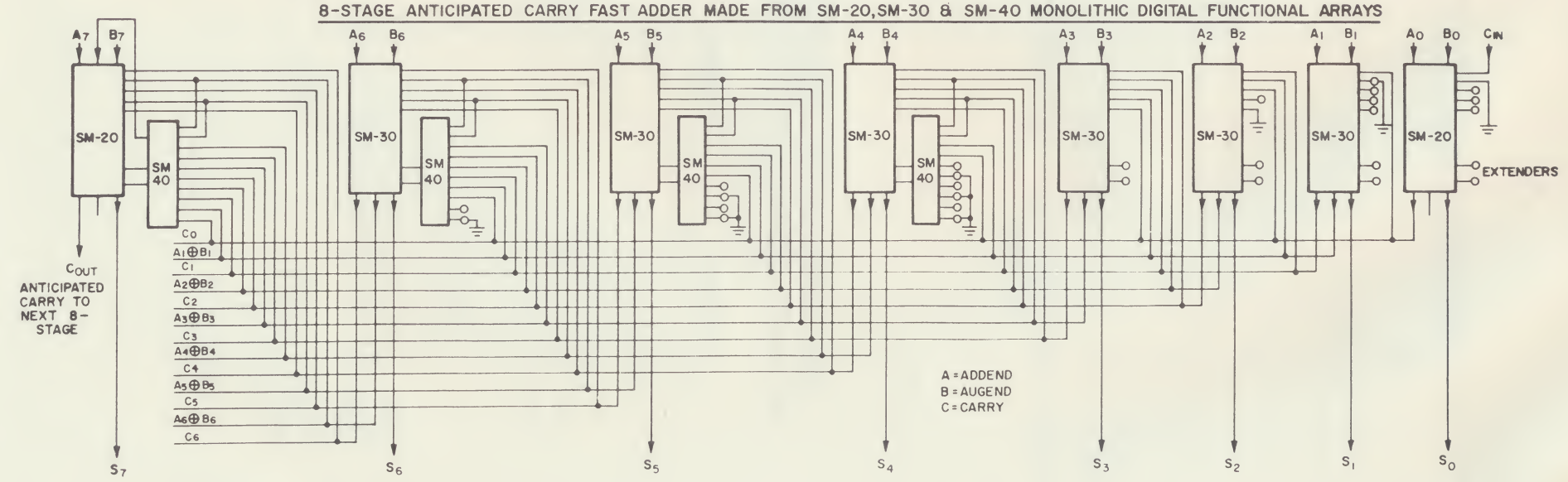


14 LEAD FLAT PACK

INTEGRATED CIRCUIT GATING STRUCTURE FOR 8-STAGE FAST ADDER



8-STAGE ANTICIPATED CARRY FAST ADDER MADE FROM SM-20, SM-30 & SM-40 MONOLITHIC DIGITAL FUNCTIONAL ARRAYS



INTEGRATED CIRCUITS

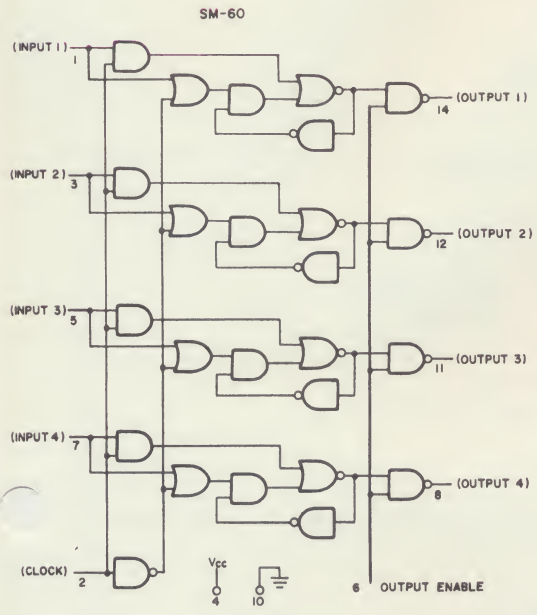
SYLVANIA

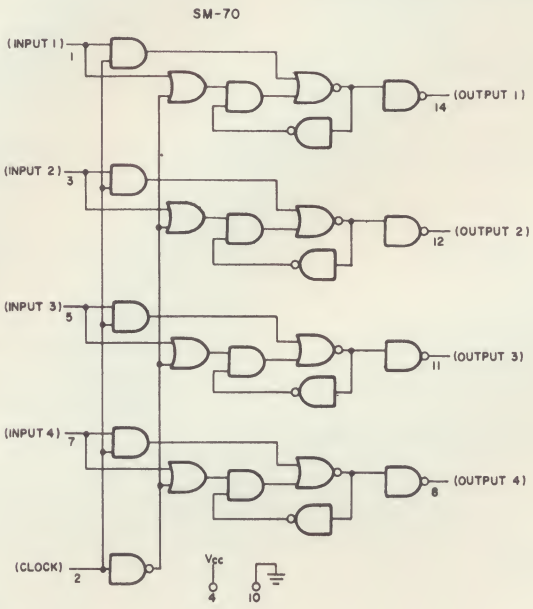
NEW PRODUCT REPORT

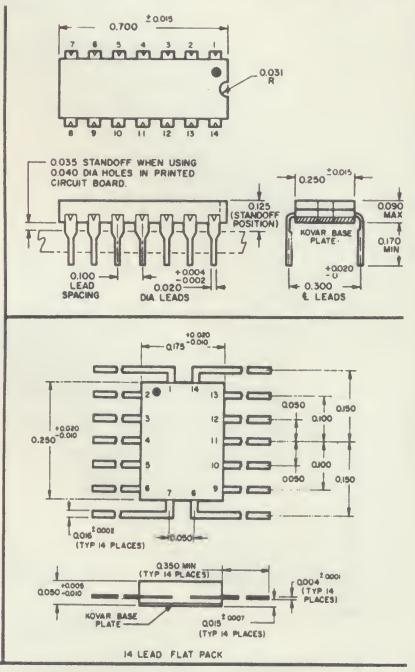
Four Bit Storage Register

SM60, SM70 Series

monolithic digital functional arrays







14 LEAD FLAT PACK

FUNCTIONAL DESCRIPTION:

The SM60 and SM70 four-bit storage register family provides high speed register subsystem functions on a single 45 by 103 mil silicon chip at low power with excellent noise immunity and high output drive capability.

Each package contains four flip-flops which are set or reset (output ="1"or"0") based on a single data input to each flip-flop and the presence of a clock pulse. If the data is a "1" the clock will allow this "1" to be stored. If the data is a "0" the clock will allow this "0" to be stored. Each flip-flop is separated from other flip-flops in the package, and data input or storage in the stage does not affect the others. The clock is common to all flip-flops.

Each stage in the four-bit storage register consists of a latching circuit having SUHL input characteristics. The latching circuit can be set only when the clock is at logic"1". The data which is permitted to enter at this time will be stored at the output when the clock returns to zero.

The SM70 output results directly from the clock pulse. The SM70 has the standard SUHL active pullup network for driving high capacitance loads. This type storage register is most useful for storing output from counters, shift registers and adders.

The SM60 is similiar to the SM70 except that SM60 output is normally a "1" regardless of the data clocked in and stored. Data clocked in is stored but is not transferred until the output is "enabled". When a logic "1" is applied to the "enable" terminal the stored data can be non-destructively read out. The output circuit for the SM60 does not have active pullup network, therefore groups of outputs can be tied together for transfer to a common buss (the "wired OR" function). The "enable" terminal can also be used as a "scan" input where large numbers of packages are used as memories or as a "strobe" signal to authorize data transfer to a buss. The output of the individual flip-flops is high when the enable pulse is at logic "0", therefore present no load to the buss.

Both Monolithic Digital Functional Arrays are designed to be used at clock rates of up to 20 mc, The clock pulse may be as narrow as 20 nsec. The data should be present at the time the clock goes to high, but going from "0" to "1" may change as close as 15 ns to the locking or negative edge of the clock and still be recognized. Data going from "1"to"0" can change up to 5 ns before the locking edge. In either case, the data must remain stable up to and including the locking edge of the clock.

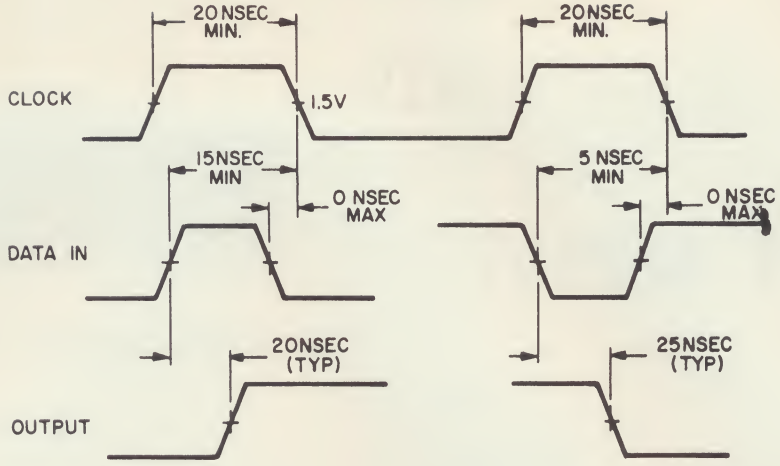
Both the SM60 and SM70 can be operated with the clock high. The output data will follow the input data during this time. Storage of data can be achieved at any point by bringing the clock low.

Data appears at the output approximately 20 ns after the input data appears and the clock is high.

The clock input typically represents four SUHL gate loads. A data input represents 2.5 typical SUHL gates.

The purpose of this report is to provide tentative engineering data on Sylvania Integrated Circuits.

TIMING SEQUENCE SM-60,SM-70



SPECIAL FEATURES:

- Four bit parallel read-in, read-out.
- High transfer rate.
- Wired OR capability (SM60)
- High capacitive drive (SM70)
- Separate clock terminal.
- Separate enable terminal.
- Available in 14-lead dual in-line plug-in package and TO85 flat pack.
- Saturated logic.
- Single five volt power supply.
- Excellent noise immunity.
- High logic levels.
- Low power consumption.
- Complete SUHL compatibility.

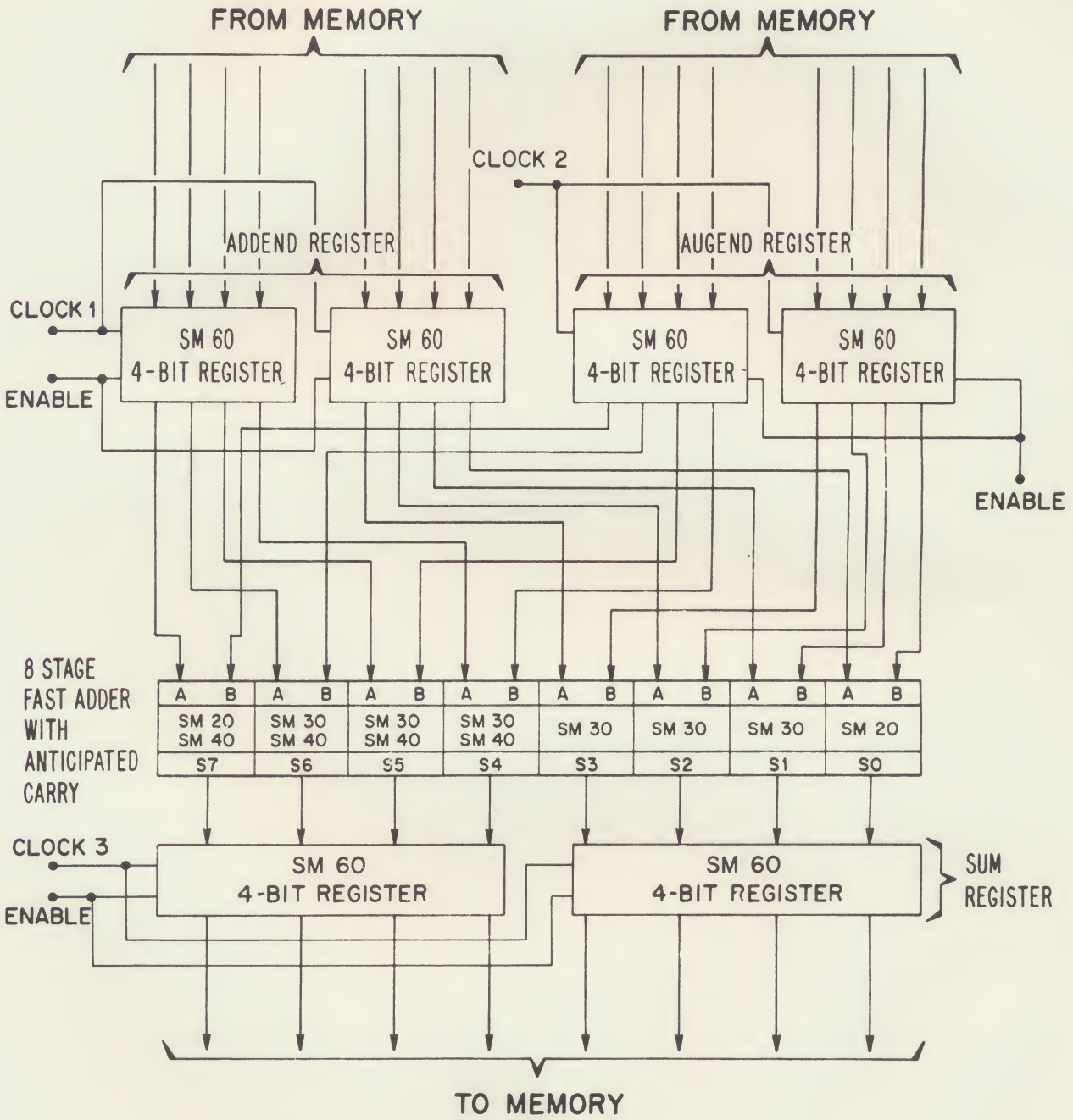
PERFORMANCE CHARACTERISTICS:

CHARACTERISTICS	TYPICAL VALUES
Output Current	20 ma.
Noise Immunity	±1.0 volt
Max. Frequency	20 mc.
Store "0"	25 ns.
Store "1"	20 ns.
Power Drain	30 mw/bit
Power Supply	5.0 volt
Input Thresholds	"0" = 1.2 v, "1" = 1.5 v
Logic Levels Output	"0" = 0.25 v, "1" = 3.3 v
Input Loading	Data = 2.9 ma. Clock = 4.4 ma. Enable (SM60 only) = 4.4 ma.
Operating Temperature	-55°C to +125°C (SM60, 61; SM70, 71) 0°C to +75°C (SM62, 63; SM72, 73)

APPLICATION AREAS:

- All main frame digital computer registers.
- Temporary storage registers.
- Crosstalk buffer storage
- Peripheral equipment buffer storage.
- A-to-D assembly storage.
- Status registers.
- Digital quantization registers.
- Output display registers.
- Scratch pad memories.

4/15/66

EIGHT STAGE CENTRAL COMPUTER
ARITHMETIC SECTION IN 18 PACKAGES

A=ADDEND B=AUGEND S=SUM